# High Efficiency, Synchronous 3A Buck Charger for 1 cell Li-ion Battery with NVDC Power Path Management

## 1 DESCRIPTION

The SC89601(D) is a 1.5MHz highly integrated switch-mode buck charger for 1 cell Li-ion battery applications and NVDC system power path management, which separate the system load and charge current, also the system can power up with deep depletion battery. System can get the power from VBUS, VBAT or both. It supports 3.9-13.5V input voltage, up to 3A charging current and provide battery charge management functions including trickle charge, constant current charge, constant voltage charge, charge termination, auto recharge and charging status indication.

The SC89601(D) supports flexible charge current option, the user can program the current and all others charger spec by I2C. With the charger management function, the IC can be used to charge 1 cell Li-ion battery.

The SC89601(D) supports USB OTG with up to 1.2A output with PFM/PWM mode. Meanwhile, the SC89601D supports USB BC1.2 and non-standard adapters.

The SC89601(D) supports input current and voltage limit, input under voltage and over voltage protections, internal cycle by cycle current limit, battery short circuit protection, and output over voltage protection. It also offers charging safety timer and over temperature protection to ensure safety under different abnormal conditions.

The SC89601(D) integrated all MOSFETs, current sensing, loop compensation and I2C interface. The SC89601(D) is available in QFN(24)-4*4 package.

## 2 FEATURES

- Integrated Synchronous Buck Charger
- Integrated NVDC Power Path Management
- Charging Management (Trickle Charge / Constant Current Charge / Constant Voltage Charge / Charge Termination)
- Integrated I2C Interface
- I2C Programmable Constant Charge Current, ±5% @720mA-3A Accuracy
- I2C Programmable Constant Voltage,±0.5% Accuracy
- I2C Programmable Charge Safety Timer
- Support OTG Discharging Function and Programmable Output Voltage: 3.9V-5.4V with up 1.2A Current
- Support Shipping Mode, Low Battery Leakage Current
- Charge Status Indication
- NTC for Battery Protection (Support JEITA Standard)
- Input Under Voltage and Over Voltage Protection
- Internal Cycle by Cycle Over Current Protection
- OTG OCP/OVP/VBATLOW Protection
- Battery Over Voltage and Short Protection
- Battery Discharging Over Current and Under Voltage Protection
- Thermal Regulation and Shutdown
- QFN(24)-4*4 Footprint

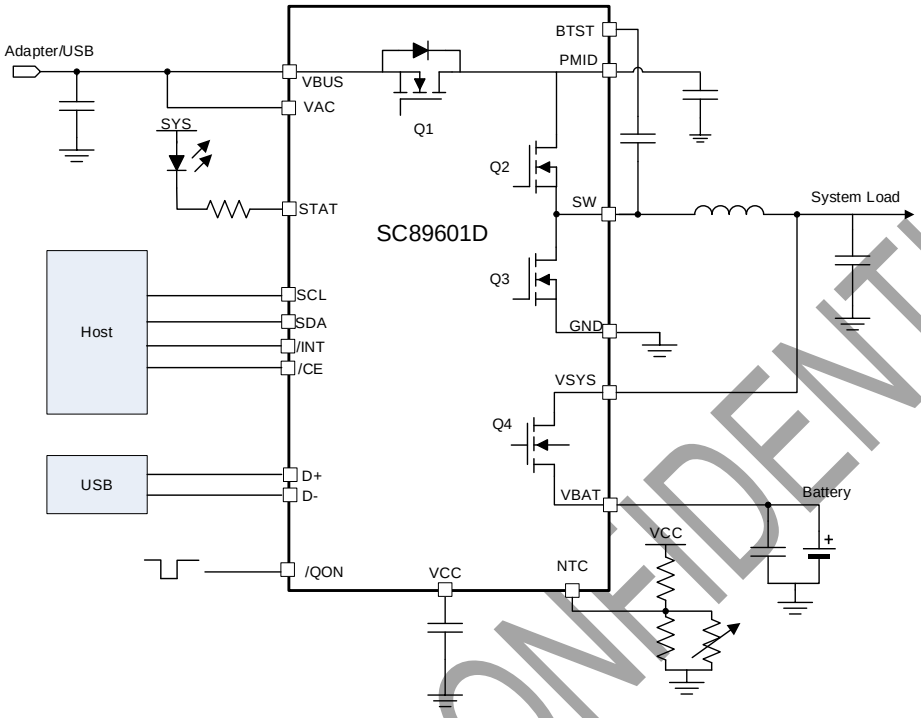
## 3 APPLICATIONS

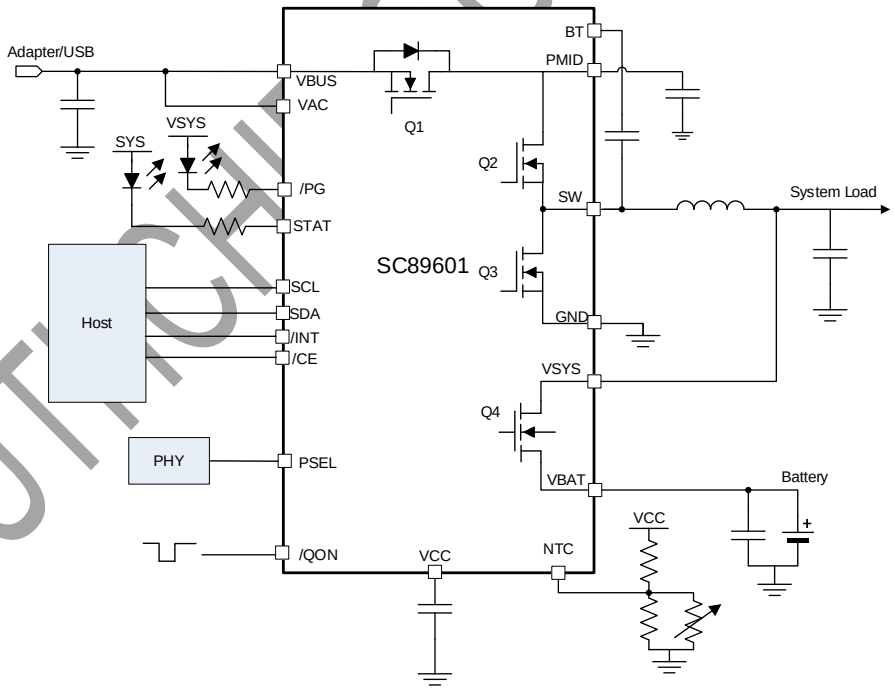
- Smart Phones
- Portable Internet Devices and Accessory

## 4 DEVICE INFORMATION

| Part Number | Package | Dimension |
|---|---|---|
| SC89601DQDLR | QFN(24)-4*4 | 4mmx4mm |
| SC89601QDLR | QFN(24)-4*4 | 4mmx4mm |

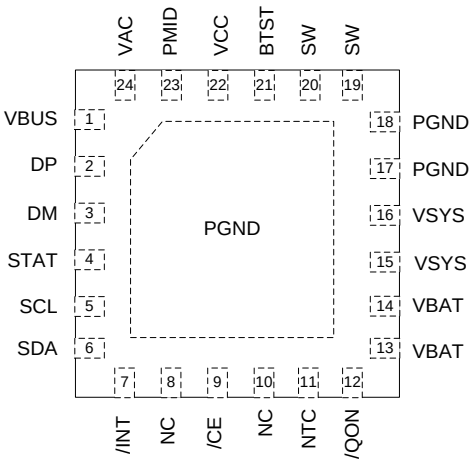
# 5 Typical Application Circuit



# 6 Terminal Configurations and Functions

**QFN(24) 4x4 (TOP View, SC89601D)**

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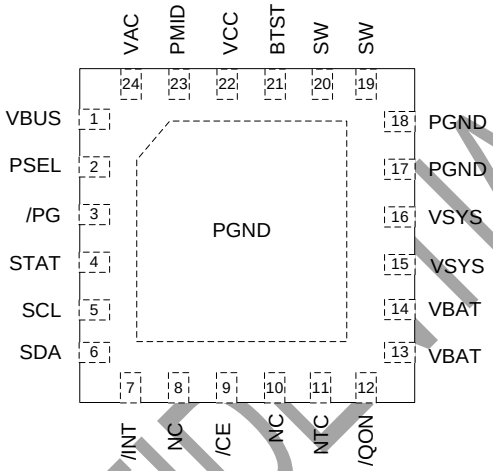



| I/O | | | | DESCRIPTION |
|---|---|---|---|---|
| SC89601D | SC89601 | NAME | | |
| 1 | 1 | VBUS | I | Power supply pin. Place a 1uF ceramic capacitor from VBUS to GND close to the IC |
| 2 | — | DP | IO | Positive line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2. |
| 3 | — | DM | IO | Negative line of the USB data line pair. DP/DM based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2. |
| — | 2 | PSEL | I | Power source selection input. Set 500 mA input current limit by pulling this pin high and set 2.4A input current limit by pulling this pin low. Once the device gets into host mode, the host can program different input current limits to IINDPM register. |
| — | 3 | /PG | O | Open drain active low power good indicator. Connect to the pull up rail through 10-kΩ resistor. LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA. |
| 4 | 4 | STAT | O | Open-drain charge status output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Collect a current limit resister and a LED from a rail to this pin.<br>Charge in progress: LOW<br>Charge complete, charger in SLEEP mode and charger disable: HIGH<br>Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses<br>This pin can be disabled via EN_STAT_PIN register bits. |
| 5 | 5 | SCL | I | I2C interface clock. Connect SCL to the logic rail through a 10-kΩ resistor. |
| 6 | 6 | SDA | IO | I2C interface data. Connect SDA to the logic rail through a 10-kΩ resistor. |
| 7 | 7 | /INT | O | Open-drain interrupt Output. Connect the /INT to a logic rail through 10-kΩ resistor. The /INT pin sends an active low, 256-μs pulse to host to report charger device status and fault. |
| 8 | 8 | NC | | |
| 9 | 9 | /CE | I | Active low charge enable pin.<br>Battery charging is enabled when CHG_CFG = 1 and /CE pin = Low. /CE pin must be pulled high or low. |
| 10 | 10 | NC | | |
| 11 | 11 | NTC | IO | Connect to the Negative Temperature Coefficient (NTC) thermistor inside the battery cells to sense the battery cells temperature for protection. If not used, connect 10kΩ resistor to |

| | | | | |
|---|---|---|---|---|
| | | | | VCC and GND respectively. |
| 12 | 12 | /QON | I | BATFET enable/reset control input. When BATFET is in shipping mode, a logic low of $t_{SHIPMODE}$ duration turns on BATFET to exit shipping mode. When VBUS is not plugged in, a logic low of $t_{QON\_RST}$ (minimum 8 s) duration resets SYS (system power) by turning BATFET off for $t_{BATFET\_RST}$ (minimum 250ms) and then re-enable BATFET to provide full system power reset. The pin contains an internal pull-up to maintain default high logic. |
| 13,14 | 13,14 | VBAT | O | Battery connection point to the positive terminal of the battery pack. Connect a 10uF ceramic capacitor close to the VBAT pin. |
| 15,16 | 15,16 | VSYS | O | Converter output connection point. Connect a 20 µF capacitor close to the VSYS pin. |
| 17,18 | 17,18 | PGND | I | Power ground pin. |
| 19,20 | 19,20 | SW | O | Switching node output. Connected to output inductor. Connect the 47nF bootstrap capacitor from SW to BTST. |
| 21 | 21 | BTST | IO | PWM high side driver positive supply. Internally, the BTST pin is connected to the cathode of the boost-strap diode. Connect the 47nF bootstrap capacitor from SW to BTST. |
| 22 | 22 | VCC | O | HSFET and LSFET driver and internal supply output. Internally, VCC is connected to the anode of the boost-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from VCC to GND. The capacitor should be placed close to the IC. |
| 23 | 23 | PMID | O | Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND. |
| 24 | 24 | VAC | I | Charge input voltage sense. This pin must be connected to VBUS pin. |

# 7 Specification

## 7.1 Absolute Maximum Rating

Over operating free-air temperature range (unless otherwise noted) (1)

| | | Min. | Max. | Unit |
|---|---|---|---|---|
| Voltage(2) | VBUS, VAC | -0.3 | 21 | V |
| | PMID | -0.3 | 21 | V |
| | BTST | -0.3 | 21 | V |
| | SW(3) | -2(10ns) | 16 | V |
| | BTST to SW | -0.3 | 6 | V |
| | DP,DM,PSEL,/PG,VCC,NTC,/CE,VBAT,VSYS,SDA,SCL,/INT,/QON,STAT | -0.3 | 6 | V |
| $T_J$ | Operating junction temperature | -40 | 150 | °C |
| $T_{stg}$ | Storage temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.
(2) All voltages are with respect to network ground terminal.
(3) SW stress test need to force DCDC off.

## 7.2 Thermal Information

| THERMAL RESISTANCE(1) | | QFN (4mmX4mm) | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction to ambient thermal resistance | 37 | °C/W |
| $\theta_{JC}$ | Junction to case resistance | 26 | °C/W |

(1) Measured on JESD51-7, 4-layer PCB.

## 7.3 ESD Ratings

| | | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{ESD}$(1) | Human-body Model (HBM) (2) | All pins | -2 | +2 | kV |
| | ChargeDMdevice Model (CDM) (3) | | -750 | +750 | V |

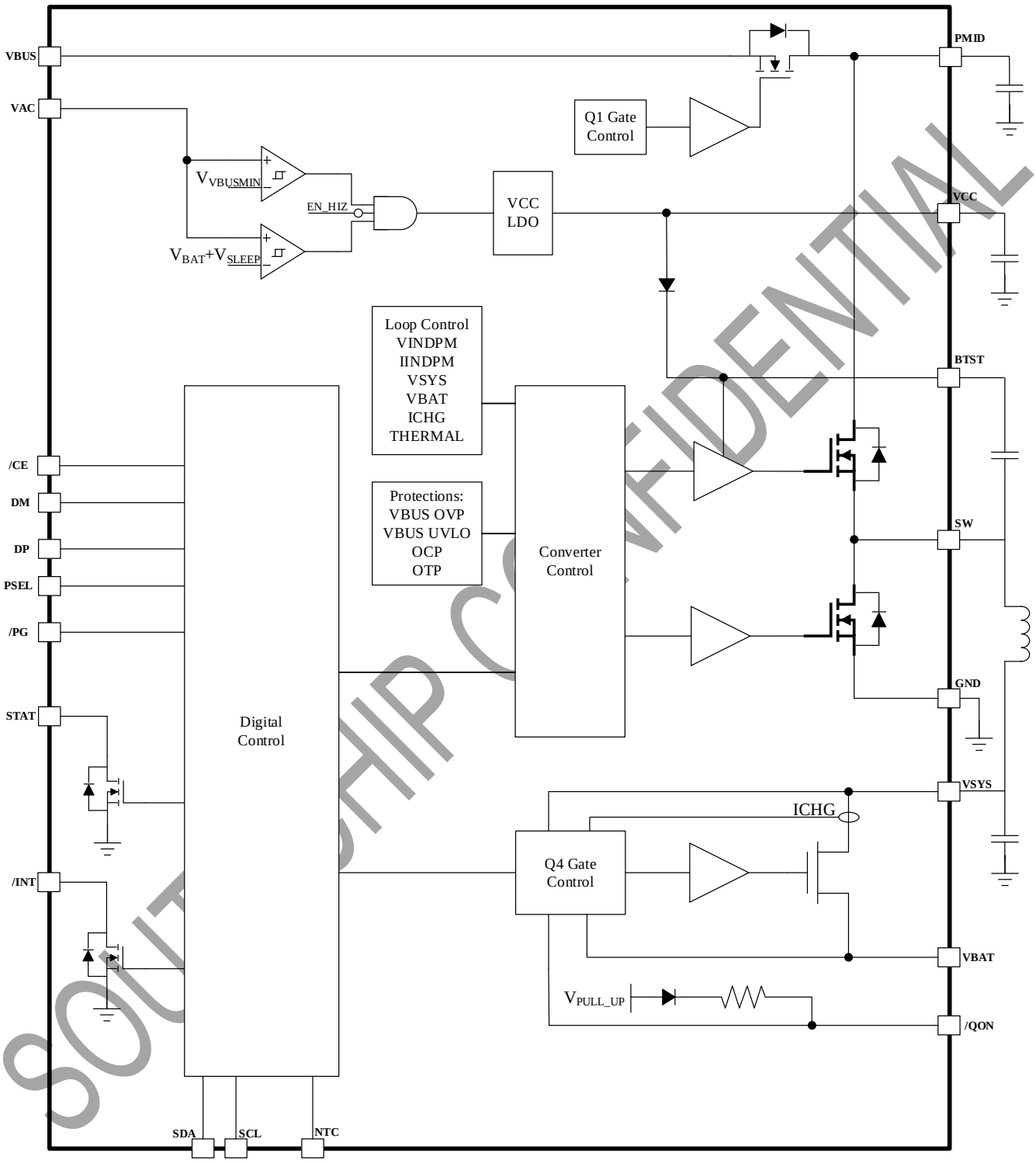
(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.4 Recommended Operation Conditions

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{BUS}$ | VBUS voltage range | 3.9 | | 13.5 | V |
| $V_{BAT}$ | VBAT voltage range | | 4.2 | 4.864 | V |
| $I_{IN}$ | Input current limit | | | 3.2 | A |

| | | | | | |
|---|---|---|---|---|---|
| $I_{CC}$ | Constant current charge current（SW Output Current） | | | 3.25 | A |
| $I_{DIS}$ | Discharging current (continue) | 6 | | | A |
| | Discharging current (100us) | 10 | | | A |
| L | Inductance | | 1 | | μH |
| $T_A$ | Operating ambient temperature | -40 | | 85 | °C |
| $T_J$ | Operating junction temperature | -40 | | 125 | °C |

# 8 Function Block Diagram



# 9 Electrical Characteristics

$T_J$= -40°C to 85 °C and $V_{AC\_UVLO}$< $V_{BUS}$ < $V_{VAC\_OVP}$, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| $V_{BUS}$ | Operating input $V_{BUS}$ voltage | | 3.9 | | 13.5 | V |
| $V_{VAC\_UVLO}$ | $V_{BUS}$ for active I2C, no battery | Rising edge | | 3.3 | 3.8 | V |
| | | Hysteresis | | 300 | | mV |
| $V_{SLEEP}$ | $V_{BUS}$-$V_{BAT}$ threshold | Falling edge | 20 | 150 | 250 | mV |
| | | Rising edge | 120 | 220 | 300 | mV |
| $V_{VAC\_OVP}$ | $V_{BUS}$ Over Voltage threshold | 5.8V, Rising edge | 5.4 | 5.8 | 6.1 | V |
| | | Hysteresis | | 300 | | V |
| | | 6.4V, Rising edge | 6.1 | 6.4 | 6.75 | V |
| | | Hysteresis | | 300 | | mV |
| | | 11V, Rising edge | 10.4 | 10.9 | 11.5 | V |
| | | Hysteresis | | 300 | | mV |
| | | 14V, Rising edge | 13.5 | 14.2 | 14.9 | V |
| | | Hysteresis | | 330 | | mV |
| $V_{VBAT\_UVLO}$ | BAT for active I2C, no VBUS | Rising edge | 2.25 | | | V |
| | | Hysteresis | | 230 | | mV |
| $V_{VBAT\_DPL}$ | Battery Depletion threshold | Falling edge | 2.5 | | 2.75 | V |
| | | Hysteresis | | 200 | | mV |
| $V_{VBUSMIN}$ | Bad adapter detection threshold | Falling edge | 3.6 | 3.7 | 3.8 | V |
| | | Hysteresis | | 200 | | mV |
| $I_{BADSRC}$ | Bad adapter detection sink current from $V_{BUS}$ to GND | | | 30 | | mA |
| $I_{BAT}$ | Battery discharge current in Buck mode | $V_{BAT}$ = 4.5 V, $V_{BUS}$ < $V_{VAC\_UVLO}$, leakage between VBAT and VBUS, $T_J \le 85°C$ | | | 5 | uA |
| | | $V_{BAT}$ = 4.5 V, HIZ mode, no $V_{BUS}$, BATFET_DIS Enable,$T_J \le 85°C$ | | 12 | 20 | uA |
| | | $V_{BAT}$ = 4.5 V, HIZ mode, no $V_{BUS}$, BATFET_DIS Disable, $T_J \le 85°C$ | | 18 | 25 | uA |
| $I_{VBUS\_HIZ}$ | Input supply current in buck mode when HIZ mode is enabled | $V_{BUS}$=5V, HIZ mode and BATFET _DIS Disable, no battery | | | 40 | uA |
| | | $V_{BUS}$=12V, HIZ mode and BATFET _DIS Disable, no battery | | | 75 | uA |
| $I_{VBUS}$ | Input supply current in buck mode | $V_{BUS}$ > $V_{VAC\_UVLO}$, $V_{BUS}$>$V_{BAT}$, Converter not switching | | 1.5 | 3 | mA |
| | | $V_{BUS}$ > $V_{VAC\_UVLO}$, $V_{BUS}$>$V_{BAT}$, Converter switching, $V_{BAT}$=3.8V, $I_{SYS}$=0A，disable charger | | 3 | | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| $I_{BOOST}$ | Battery discharge current in boost mode | $V_{BAT}$=4.2V, boost mode, $I_{BUS}$=0A, converter switching | | | 3 | mA |
| **POWER PATH** | | | | | | |
| $V_{SYS}$ | Typical system regulation voltage | $I_{SYS}$=0A,$V_{BAT}$<$V_{SYSMIN}$,$I_{SYS}$=0A, BATFET Disable | | $V_{SYSMIN}$+2 50mV | | V |
| | | $I_{SYS}$=0A,$V_{BAT}$>$V_{SYSMIN}$,$I_{SYS}$=0A, BATFET Disable | | $V_{BAT}$+50 mV | | V |
| $V_{SYS\_MIN}$ | Minimum system regulation voltage | $V_{VBAT}$ <SYS_MIN[2:0] = 101(3.5V), BATFET Disabled | | 3.75 | | V |
| | | Range | 2.6 | | 3.7 | V |
| $V_{SYS\_MAX}$ | Maximum DC system voltage output | $I_{SYS}$=0A,$V_{BAT}$>$V_{SYSMIN}$,$I_{SYS}$=0A, BATFET Disable, $V_{BAT}$<=4.4V | 4.4 | 4.45 | 4.51 | V |
| $R_{DSON\_Q1}$ | Reverse blocking MOSFET on resistance | Pin to Pin | | 40 | 45 | mΩ |
| $R_{DSON\_Q2}$ | High side switching MOSFET on resistance | $V_{CC}$=5V, Pin to Pin | | 65 | 70 | mΩ |
| $R_{DSON\_Q3}$ | Low side switching MOSFET on resistance | $V_{CC}$=5V, Pin to Pin | | 68 | 73 | mΩ |
| $R_{DSON\_Q4}$ | $V_{SYS}$ to $V_{BAT}$ MOSFET on resistance | $V_{VBAT}$=4.2V, Pin to Pin | | 28 | 36 | mΩ |
| $V_{FWD}$ | Supplement mode Q4 forward voltage | | | 30 | | mV |
| **CHARGER MANAGEMENT** | | | | | | |
| $V_{BATREG\_RANGE}$ | Regulation Charge Voltage | | 3.848 | | 4.864 | V |
| $V_{BATREG\_STEP}$ | Charge Voltage step | | | 8 | | mV |
| $V_{BATREG}$ | Charge Voltage | VREG = 4.2V | 4.179 | 4.2 | 4.221 | V |
| | | VREG = 4.344V | 4.321 | 4.344 | 4.365 | V |
| | | VREG = 4.128V | 4.107 | 4.128 | 4.15 | V |
| | | VREG = 4.384V | 4.362 | 4.384 | 4.4 | V |
| | | VREG = 4.432V | 4.41 | 4.432 | 4.45 | V |
| $I_{CC\_RANGE}$ | Constant charging current range | | 0 | | 3 | A |
| $I_{CC\_STEP}$ | Constant charging current step | | | 60 | | mA |
| $I_{CC}$ | Constant charging current | $I_{CC}$=240mA, $V_{VBAT}$=3.1V-3.8V | 0.216 | 0.24 | 0.264 | A |
| | | $I_{CC}$=720mA, $V_{VBAT}$=3.1V-3.8V | 0.685 | 0.72 | 0.756 | A |
| | | $I_{CC}$=1.38A, $V_{VBAT}$=3.1V-3.8V | 1.311 | 1.38 | 1.449 | A |
| | | ICC=2.04A, VVBAT=3.1V-3.8V | 1.938 | 2.04 | 2.142 | A |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{TC}$ | Trickle charge to CC Charge battery voltage threshold | 3V, Rising edge | 2.9 | 3 | 3.1 | V |
| | | Hysteresis | | 200 | | mV |
| | | 2.8V, Rising edge | 2.7 | 2.8 | 2.9 | V |
| | | Hysteresis | | 300 | | mV |
| $I_{TC}$ | Trickle charge current | Step | | 60 | | mA |
| | | Range | 60 | | 960 | mA |
| | | $I_{TC}$=120mA | 90 | 120 | 150 | mA |
| | | $I_{TC}$=180mA | 150 | 180 | 207 | mA |
| | | $I_{TC}$=420mA | 390 | 420 | 450 | mA |
| $I_{TERM}$ | Termination current | Step | | 60 | | mA |
| | | Range | 60 | | 960 | mA |
| | | $I_{TC}$=120mA | 90 | 120 | 150 | mA |
| | | $I_{TC}$=180mA | 162 | 180 | 198 | mA |
| | | $I_{TC}$=420mA | 390 | 420 | 450 | mA |
| $V_{BAT\_SHORT}$ | Battery short voltage | Falling edge | 1.85 | 2 | 2.15 | V |
| | | Hysteresis | | 200 | | mV |
| $I_{SHORT}$ | Battery short charge current | $V_{BAT}$<$V_{BAT\_SHORT}$, 90mA | 70 | 90 | 110 | mA |
| | | $V_{BAT}$<$V_{BAT\_SHORT}$, 50mA | 35 | 50 | 65 | mA |
| $V_{RECHG}$ | Recharge threshold below $V_{BAT\_REG}$ | $V_{BAT}$ falling edge,100mV | 70 | 100 | 130 | mV |
| | | $V_{BAT}$ falling edge, 200mV | 170 | 200 | 230 | mV |
| $I_{SYSLOAD}$ | System discharge load current | $V_{SYS}$=4.2V | | 30 | | mA |
| $t_{TERM\_DGL}$ | Deglitch time for charge termination | | | 250 | | ms |
| $t_{RECH\_DGL}$ | Deglitch time for recharge | | | 250 | | ms |
| $t_{BATOCP\_DGL}$ | Battery over-current(10A) deglitch time to turn off Q4 | | | 100 | | us |
| $t_{SYSOVP\_DGL}$ | System over-voltage deglitch time to turn off DCDC | | | 1 | | us |
| $t_{BATOVP\_DGL}$ | Battery over-voltage deglitch time to disable charger | | | 1 | | us |
| **INPUT VOLTAGE AND CURRENT REGULATION** | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{INDPM}$ | Input voltage regulation limit | Range | 3.9 | | 8.4 | V |
| | | Step | | 100 | | mV |
| | | Accuracy | -3 | | +3 | % |
| $V_{INDPM\_VBAT}$ | Input voltage regulation limit tracking VBAT | $V_{BAT}$=4V, $V_{DPM\_VBAT\_TRACK}$=300mV | 4.171 | 4.3 | 4.43 | V |
| $I_{INDPM}$ | USB input current regulation limit | Range | 100 | | 3200 | mA |
| | | Step | | 100 | | mA |
| | | $V_{VBUS}$=5V, $I_{INDPM}$=500mA | 450 | 470 | 500 | mA |
| | | $V_{VBUS}$=5V, $I_{INDPM}$=900mA | 750 | 825 | 900 | mA |
| | | $V_{VBUS}$=5V, $I_{INDPM}$=1.5A | 1.3 | 1.4 | 1.5 | A |
| | | $V_{VBUS}$=5V, $I_{INDPM}$=2.4A | 2.2 | 2.3 | 2.4 | A |
| $I_{IN\_START}$ | Input current limit during system start-up sequence | | | 200 | | mA |
| **PROTECTION** | | | | | | |
| $V_{VBAT\_OVP}$ | Battery over voltage threshold | Rising | 103 | 104 | 105 | % |
| | | Hysteresis | | 2 | | % |
| $I_{BATOCP}$ | Battery discharge over current threshold | 100μs deglitch | 10 | | | A |
| **PWM** | | | | | | |
| $f_{SW}$ | PWM switching frequency | VBUS= 9V，VBAT=4V，Icc= 2A | 1320 | 1500 | 1680 | kHz |
| $D_{MAX}$ | Maximum PWM duty cycle(Buck) | | | 97 | | % |
| **JEITA (BUCK MODE)** | | | | | | |
| $V_{COLD}$ | NTC cold temp (0°C) threshold | Rising | 72.3 | 73.3 | 74.3 | % |
| | | falling | 71 | 72 | 73 | % |
| $V_{COOL}$ | NTC cool temp threshold | 5°C Rising | 69.75 | 70.75 | 71.75 | % |
| | | 5°C falling | 68.2 | 69.2 | 70.2 | % |
| | | 10°C Rising | 67.25 | 68.25 | 69.25 | % |
| | | 10°C falling | 65.95 | 66.95 | 67.95 | % |
| | | 15°C Rising | 64.25 | 65.25 | 66.25 | % |
| | | 15°C falling | 63.2 | 64.2 | 65.2 | % |
| | | 20°C Rising | 61.25 | 62.25 | 63.25 | % |
| | | 20°C falling | 60.2 | 61.2 | 62.2 | % |
| $V_{WARM}$ | NTC warm temp threshold | 40°C Falling | 47.25 | 48.25 | 49.25 | % |
| | | 40°C Rising | 48.3 | 49.3 | 50.3 | % |
| | | 45°C Falling | 43.75 | 44.75 | 45.75 | % |
| | | 45°C Rising | 44.8 | 45.8 | 46.8 | % |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | 50°C Falling | 39.7 | 40.7 | 41.7 | % |
| | | 50°C Rising | 40.8 | 41.8 | 42.8 | % |
| | | 55°C Falling | 36.7 | 37.7 | 38.7 | % |
| | | 55°C Rising | 38 | 39 | 40 | % |
| $V_{HOT}$ | NTC hot temp (60°C) threshold | Falling | 33.2 | 34.2 | 35.2 | % |
| | | Rising | 34.3 | 35.3 | 36.2 | % |
| $I_{RATIO\_COOL}$ | ICC Ration during JEITA COOL | REG05[0]=1, REG0C[7]=1 | | 0 | | % |
| | | REG05[0]=1, REG0C[7]=0 | | 20 | | % |
| | | REG05[0]=0, REG0C[7]=0 | | 50 | | % |
| | | REG05[0]=0, REG0C[7]=1 | | 100 | | % |
| $I_{RATIO\_WARM}$ | ICC Ration during JEITA WARM | REG0C[5:4]=00 | | 0 | | % |
| | | REG0C[5:4]=01 | | 20 | | % |
| | | REG0C[5:4]=10 | | 50 | | % |
| | | REG0C[5:4]=11 | | 100 | | % |
| $V_{DELTA\_WARM}$ | VBAT Regulation Voltage during JEITA WARM | REG07[4]=1, REG0C[6]=0 | | 0 | | mV |
| | | REG07[4]=1, REG0C[6]=1 | | 50 | | mV |
| | | REG07[4]=0, REG0C[6]=1 | | 100 | | mV |
| | | REG07[4]=0, REG0C[6]=0 | | 200 | | mV |
| **NTC (BOOST MODE)** | | | | | | |
| $V_{BCOLD}$ | NTC cold temp threshold | Rising | 79 | 80 | 81 | % |
| | | falling | 78 | 79 | 80 | % |
| $V_{BHOT}$ | NTC hot temp threshold | Falling | 30.2 | 31.2 | 32.2 | % |
| | | Rising | 33.2 | 34.2 | 35.2 | % |
| **BOOST MODE OPERATION** | | | | | | |
| $V_{OTG\_REG}$ | Boost mode regulation voltage, controlled by BOOSTV[0:4] | Range | 3.9 | | 5.4 | V |
| | | Step | | 100 | | mV |
| | | Accuracy, $I_{VBUS}$=0A | -3 | | +3 | % |
| $V_{BATLOW\_OTG}$ | Battery voltage exiting boost mode | $V_{BAT}$ falling,2.8V | 2.7 | 2.8 | 2.9 | V |
| | | Hysteresis | | 200 | | mV |
| | | $V_{BAT}$ falling, 2.5V | 2.4 | 2.5 | 2.6 | V |
| | | Hysteresis | | 300 | | mV |
| BOOST_LIM | OTG mode output current limit | BOOST_LIM = 1.2A | 1.2 | 1.4 | 1.6 | A |
| | | BOOST_LIM = 0.5A | 0.5 | 0.6 | 0.72 | A |
| $V_{OTG\_OVP}$ | OTG overvoltage threshold | Rising | 5.8 | 6 | 6.15 | V |
| **VCC LDO** | | | | | | |
| $V_{VCC}$ | $V_{CC}$ LDO output voltage | $V_{BUS}$=9V, $I_{VCC}$=40mA | | 5 | | V |
| | | $V_{BUS}$=5V, $I_{VCC}$=20mA | | 4.7 | | V |
| $I_{VCC}$ | $V_{CC}$ current limit | VBUS=5V, $V_{VCC}$ = 3.8V, Charger disable | 50 | | | mA |

| | | | | | | |
|---|---|---|---|---|---|---|
| **LOGIC IO** | | | | | | |
| $V_{ILO}$ | Input low threshold | | | | 0.4 | V |
| $V_{IHO}$ | Input high threshold | | 0.9 | | | V |
| **/QON TIMING** | | | | | | |
| $t_{SHIPMODE}$ | /QON low time to turn on BATFET and exit ship mode | | 0.9 | | 1.3 | s |
| $t_{QON\_RST}$ | /QON low time to reset BATFET | | 8 | | 12 | s |
| $t_{BATFET\_RST}$ | BATFET off time during full system reset | | 250 | | 450 | ms |
| $t_{SHIPMODE\_DLY}$ | Enter ship mode delay | | 8 | | 15 | s |
| **DIGITAL CLOCK AND WATCHDOG TIMER** | | | | | | |
| $t_{WDT}$ | Watchdog timer | | | 40 | | s |
| $f_{SCL}$ | SCL Clock frequency | | | | 400 | kHz |
| **SAFETY TIMER** | | | | | | |
| $t_{TC}$ | Safety timer for Trickle charge | | | 2 | | hours |
| $t_{CC/CV}$ | Safety timer for CC and CV | | | 10 | | hours |
| $t_{TOP\_OFF}$ | Top-Off timer | Range | 0 | | 45 | min |
| | | Step | | 15 | | min |
| **VBUS Power up** | | | | | | |
| $t_{VAC\_OVP}$ | $V_{AC}$ OVP reaction time | | | 100 | | ns |
| $t_{BADSRC}$ | Bad adapter detection duration | | | 30 | | ms |
| **THERMAL REGULATION and SHUTDOWN** | | | | | | |
| $T_{REG}$ | Thermal regulation temperature | Temperature Increasing, TREG= 110℃ (REG05[1] = 1) | | 110 | | °C |
| | | Temperature Increasing, TREG= 90℃(REG05[1] = 0) | | 90 | | °C |
| $T_{SHUT}$ | Thermal shutdown temperature | | | 150 | | °C |
| | Thermal shutdown hysteresis | | | 30 | | °C |
| **DP/DM Detection(only for SC89601D)** | | | | | | |
| $V_{0P6\_VSRC}$ | DP/DM voltage source (0.6 V) | | 0.5 | 0.6 | 0.7 | V |
| $V_{1P2\_VSRC}$ | DP/DM voltage source (1.2 V) | | 1.1 | 1.2 | 1.3 | V |
| $V_{2P0\_VSRC}$ | DP/DM voltage source (2.0 V) | | 1.9 | 2 | 2.1 | V |
| $V_{2P7\_VSRC}$ | DP/DM voltage source (2.7 V) | | 2.6 | 2.7 | 2.8 | V |
| $V_{3P3\_VSRC}$ | DP/DM voltage source (3.3 V) | | 3.2 | 3.3 | 3.4 | V |
| $V_{0P325\_VTH}$ | DP/DM Input comparator threshold | | 0.25 | | 0.4 | V |
| $V_{1P0\_VTH}$ | DP/DM Input comparator threshold | | 0.9 | | 1.1 | V |
| $V_{1P35\_VTH}$ | DP/DM Input comparator threshold | | 1.25 | | 1.45 | V |
| $V_{2P2\_VTH}$ | DP/DM Input comparator | | 2.1 | | 2.3 | V |

| | | | | |
|---|---|---|---|---|
| | threshold | | | |
| $V_{3P0\_VTH}$ | DP/DM Input comparator threshold | | 2.9 3.1 | V |
| $I_{DP/DM\_SRC}$ | BC1.2 DP/DM source capability | 0.6V output | 250 | μA |
| | | 3.3V output | 250 | μA |
| $R_{DP/DM\_PD}$ | DP/DM pull down resistor | | 19.53 | KΩ |
| $I_{DP/DM\_SINK}$ | BC1.2 DP/DM sink current | 50μA | 50 | μA |

# 10 Feature Description

## 10.1 Power-On-Reset (POR)

The SC89601(D) powers internal bias circuits from the higher voltage of VBUS and VBAT. When VBUS rises above $V_{VBUS\_UVLO}$ or VBAT rises above $V_{VBAT\_UVLO}$, the sleep comparator, battery depletion comparator and BATFET driver are active. I2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

## 10.2 Device Power Up from Battery without Input Source

If only battery is present and the voltage is above depletion threshold, the BATFET turns on and connects battery to system. The VCC LDO stays off to minimize the quiescent current. The low $R_{DSON}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET (Supplement Mode). When the system is overloaded or shorted ($I_{BAT}$ > $I_{BATOCP}$), the device turns off BATFET immediately and set BATFET_DIS bit to indicate BATFET is disabled until the input source plugs in again or one of the methods described in BATFET Enable (Exit Shipping Mode) is applied to re-enable BATFET.

## 10.3 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on VCC LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power up VCC LDO

2. Poor Source Qualification

3. Input Source Type Detection is based on DP/DM(for SC89601D) or PSEL(for SC89601) to set default input current limit (IINDPM) register or input source type

4. Input Voltage Limit Threshold Setting (VINDPM threshold)

5. Converter Power-up

### 10.3.1 Power Up VCC LDO Regulation

The VCC LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. The VCC also provides bias rail to NTC external resistors. The pull-up rail of STAT can be connected to VCC as well. The VCC is enabled when all the below conditions are valid:

- $V_{BUS}$ above $V_{BUSMIN}$, above $V_{BAT}$ + $V_{SLEEP}$ in buck mode
- $V_{BUS}$ below $V_{BAT}$ + $V_{SLEEP}$ in boost mode
- Above conditions are satisfied during 220ms delay

If any one of the above conditions is not valid, the device is in high impedance mode (HIZ) with VCC LDO off. The device draws less than $I_{VBUS\_HIZ}$ from VBUS during HIZ state. The battery powers up the system when the device is in HIZ mode.

By setting EN_HIZ bit to 1 with adapter, the device enters high impedance state (HIZ). In HIZ mode, the system is powered from battery even with good adapter present. The device is in the low input quiescent current state with Q1 RBFET, VCC LDO and the bias circuits off.

### 10.3.2 Poor Source Qualification

After VCC LDO powers up, the device confirms the current capability of the input source. The input source must meet both of the following requirements to start the buck converter:

- VBUS voltage below $V_{VAC\_OV}$
- VBUS voltage above $V_{VBUSMIN}$ when pulling $I_{BADSRC}$ (typical 30 mA)

Once the input source passes all the conditions above, the status register bit VBUS_GD is set high and the /INT pin is pulsed to signal to the host. If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

### 10.3.3 Input Source Type Detection (For SC89601D)

After the VBUS_GD bit is set and VCC LDO is powered, the device runs input source detection through DP/DM. The SC89601(D) follows the USB Battery Charging Specification 1.2 (BC1.2) to detect input source (SDP/CDP/DCP) and non-standard adapter through USB DP/DM lines.

After input source type detection is completed, an /INT pulse is asserted to the host. In addition, the following registers and pin are changed:

1. Input Current Limit (IINDPM) register is changed to set current limit

2. PG_STAT bit is set

3. VBUS_STAT bit is updated to indicate USB or other input source

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

When AUTO_DPDM_EN is disabled, the Input Source Type Detection is bypassed.

The SC89601D contains a DP/DM based input source detection to set the input current limit when VBUS plug-in. The DP/DM detection includes standard USB BC1.2 and non-standard adapter. When input source is plugged in, the device starts standard USB BC1.2 detection. The USB BC1.2 is capable to identify Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). When the Data Contact Detection (DCD) timer expires, the nonstandard adapter detection is applied to set the input current limit. The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the DP/DM pins. If an adapter is detected as DCP, the input current limit is set at 2.4A. If an adapter is detected as unknown, the input current limit is set at 0.5A.

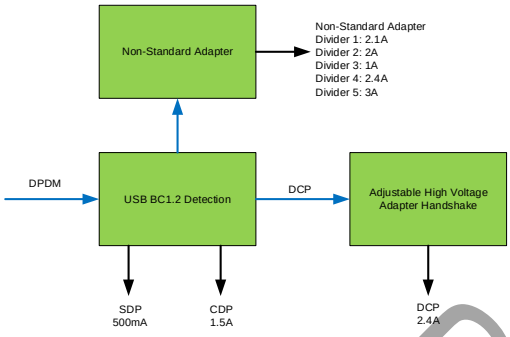



**Figure 1. USB DP/DM Detection**

| DP/DM DETECTION | INPUT CURRENT LIMIT |
|---|---|
| USB SDP | 500mA |
| USB CDP | 1.5A |
| USB DCP | 2.4A |
| Divider 1 | 2.1A |
| Divider 2 | 2A |
| Divider 3 | 1A |
| Divider 4 | 2.4A |
| Divider 5 | 3A |
| Unknown Adapter | 500mA |

**Table 1. Input current limit setting from DP/DM Detection**

After the input source detection, for SDP, CDP, DCP and Non-standard adapters, DP/DM is forced to HIZ.

### 10.3.4 Input Source Type Detection (For SC89601)

After the VBUS_GD bit is set and VCC LDO is powered, the device runs input source detection through PSEL. The SC89601 sets input current limit through PSEL pins. After input source type detection is completed, an INT pulse is asserted to the host. In addition, the following registers and pin are changed:

4. Input Current Limit (IINDPM) register is changed to set current limit

5. PG_STAT bit is set

6. VBUS_STAT bit is updated to indicate USB or other input source

The host can over-write IINDPM register to change the input current limit if needed. The charger input current is always limited by the IINDPM register.

### 10.3.5 Input Voltage Limit Threshold Setting

The SC89601(D) supports wide range of input voltage limit (3.9 V – 8.4V). For USB, VINDPM is set at 4.5V. The device supports dynamic VINDPM tracking settings which tracks the battery voltage. This function can be enabled via the VINDPM _TRACK [1:0] register bits. When enabled, the actual input voltage limit will be the higher of the VINDPM register and VBAT + VINDPM _TRACK offset.

### 10.3.6 Converter Power-Up

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. If battery charging is disabled, BATFET turns off. Otherwise, BATFET stays on to charge the battery.

The SC89601(D) provides soft-start when system rail is ramped up. When the system rail is below 2.2 V, the input current is limited to is the lower of 200 mA or IINDPM register setting. After the system rises above 2.2 V, the device limits input current to the value set by IINDPM register.

As a battery charger, the device deploys a highly efficient 1.5 MHz step-down switching regulator. The frequency oscillator keeps tight control of the switching frequency depends on conditions of input voltage, battery voltage, charge current.

The SC89601(D) switches to PFM control at light load or when battery is below minimum system voltage setting or charging is disabled.

## 10.4 Boost Mode Operation from Battery

The SC89601(D) supports boost converter operation to deliver power from the battery to other portable devices through USB port. The boost mode output current rating meets the USB On-The-Go 500 mA output requirement. The maximum output current is up to 1.2 A. The boost operation can be enabled if the conditions are valid:

1. VBAT above $V_{BATLOW\_OTG}$

2. VBUS less than VBAT + $V_{SLEEP}$

3. OTG_CFG is enabled and CHG_CFG is disabled

4. Battery is not in BCOLD and BHOT.

5. Above conditions are satisfied during 30ms delay.

During boost mode, the status register VBUS_STAT bits is set to 111, the VBUS output is 5V and the output current can reach up to 1.2 A, selected through I2C (BOOST_LIM bit). The boost output is maintained when BAT is above $V_{BATLOW\_OTG}$ threshold.

In boost mode, the device employs a 500kHz or 1.5MHz (selectable using BOOST_FREQ bit) step-up switching regulator based on system requirements. To avoid frequency change during boost mode operations, write to boost frequency configuration bit (BOOST_FREQ) is ignored when OTG_CFG is set.

## 10.5 Host Mode and Default Mode

The SC89601(D) is a host-controlled charger, but it can operate in default mode without host management. In default mode, the device can be used as an autonomous charger with no host or while host is in sleep mode.

When the charger is in default mode, WD_FAULT bit is HIGH. When the charger is in host mode, WD_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings. In default mode, the device keeps charging the battery with default 10-hour fast charging safety timer. At the end of the 10-hour, the charging is stopped and the buck converter continues to operate to supply system load.

Writing reg transitions the charger from default mode to host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer expires (WD_FAULT bit = 1), the device returns to default mode and all registers are reset to default values except IINDPM, VINDPM, BATFET_RST_EN, BATFET_DLY, and BATFET_DIS bits.

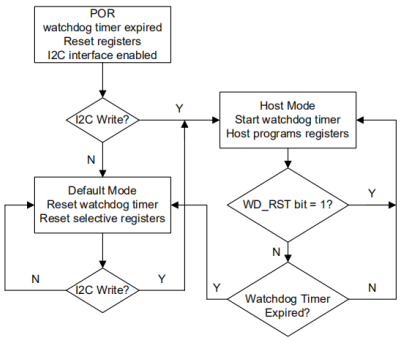



**Figure 2. Watch dog**

## 10.6 NVDC Power Path Management

The SC89601(D) accommodates a wide range of input sources from USB, wall adapter, to car charger. The device provides automatic power path selection to supply the system (VSYS) from input source (VBUS), battery (VBAT), or both.

### 10.6.1 Battery Charging Management

The SC89601(D) charges 1-cell Li-Ion battery with up to 3A charge current for high capacity battery. The low Rdson BATFET improves charging efficiency and minimize the voltage drop during discharging.

#### *10.6.1.1 Autonomous Charging Cycle*

With battery charging is enabled (CHG_CFG bit = 1 and /CE pin is LOW), the device autonomously completes a charging cycle without host involvement. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I2C.

| Charging Parameters | Default Value |
|---|---|
| Charging Voltage | 4.2V |
| CC Current | 2.04A |
| TC Current | 180mA |
| Termination Current | 180mA |
| Battery Temperature Profile | JEITA |
| Safety Timer | TC:2hours, CC/CV:10hours |

**Table 2. Charging Parameter Default Setting**

A new charge cycle starts when the following conditions are valid:

- Converter starts

- Battery charging is enabled (CHG_CFG bit =1, $I_{CC}$ is not 0A and /CE is low)
- No NTC COLD or HOT fault
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit=0)

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, battery voltage is above recharge threshold, and device not is in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggle /CE pin or CHG_CFG bit can initiate a new charging cycle. Adapter removal and re-plug in will also start a new charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). The STAT output can be disabled by setting STAT_DIS=1. in addition, the status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-trickle charge, 10-fast charge (constant current and constant voltage mode), 11-end of charger. Once a charging cycle is completed, an INT is asserted to notify the host.

| STAT status | IC working status |
|---|---|
| Low | Normal charging (TC/CC/CV/Recharge) |
| High | End of charging (EOC, top off timer maybe running), charge disable, sleep mode, Boost Mode |
| 1Hz Blinking | Charge suspend (VAC OVP, NTC COLD/HOT, Safety timer out, VBAT OVP).<br>Boost Mode suspend (NTC/COLD/HOT) |

**Table 3. STAT Pin status**

### *10.6.1.2 Battery Charging Profile*

The SC89601(D) charges the battery in five phases: battery short, TC, CC, CV, and top-off charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

| $V_{VBAT}$ | Charging current | Default value | CHRG_STAT |
|---|---|---|---|
| <2.2V | $I_{SHORT}$ | 50mA | 01 |
| 2.2V to 2.8V | $I_{TC}$ | 180mA | 01 |
| >2.8V | $I_{CC}$ | 2.04A | 10 |

**Table 4. Charging Current Setting**

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. in this case, termination is temporarily disabled and the charging safety timer is doubled.

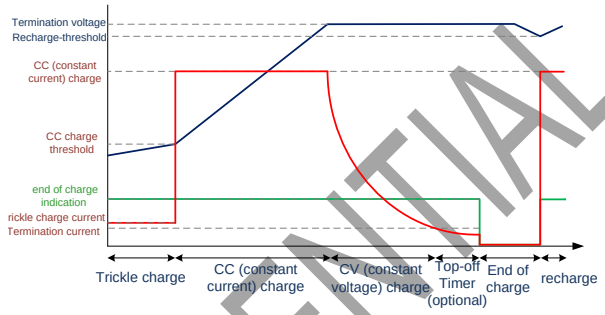



**Figure 3. Battery Charging Profile**

### *10.6.1.3 End of Charge*

The SC89601(D) terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the status register CHRG_STAT is set to 11, and an /INT pulse is asserted to the host. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

At low termination currents (60mA), due to the comparator offset, the actual termination current may be 10 mA-20 mA higher than the termination target. In order to compensate for comparator offset, a programmable top-off timer can be applied after termination is detected. The termination timer will follow safety timer constraints, such that if safety timer is suspended, so will the termination timer. Similarly, if safety timer is doubled, so will the termination timer. TOPOFF_ACTIVE bit reports whether the top off timer is active or not. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status.

Top off timer gets reset at one of the following conditions:

1. Charge disable to enable
2. Termination status low to high
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value

after termination will have no effect unless a recharge cycle is initiated. An /INT is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

#### *10.6.1.4 NTC in Buck mode*

The SC89601(D) monitors the battery cell's temperature through NTC pin. It monitors the NTC voltage. Once it detects the temperature is below 0°C or higher than 60°C, the IC will stop charging. Below shows the NTC operation summary.

| $V_{NTC}$ | Temperature | Operation |
|---|---|---|
| $V_{NTC} > V_{COLD}$ | T < 0°C | Stop charging |
| $V_{COLD} > V_{NTC} > V_{COOL}$ | 0°C < T < 10°C | 0/0.5/0.2/1 CC current |
| $V_{COOL} > V_{NTC} > V_{WARM}$ | 10°C < T < 45°C | Normal charging |
| $V_{WARM} > V_{NTC} > V_{HOT}$ | 45°C < T < 60°C | CV/CV-50m/CV-100mV/CV-200mV<br>0/0.5/0.2/1 CC current |
| $V_{NTC} < V_{HOT}$ | T > 60°C | Stop charging |

**Table 5. NTC function**

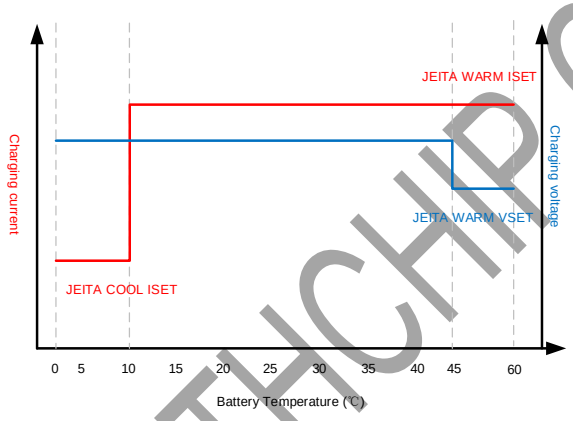



**Figure 4. NTC function**

#### *10.6.1.5 NTC in Boost mode*

For battery protection during boost mode, the SC89601(D) monitors the battery temperature to be within the $V_{BCOLD}$ to $V_{BHOT}$ thresholds. When temperature is outside of the temperature thresholds, the boost mode is suspended. In additional, VBUS_STAT bits are set to 000 and NTC_FAULT is reported. Once temperature returns within thresholds, the boost mode is recovered and NTC_FAULT is cleared.

#### *10.6.1.6 Safety Timer*

The SC89601(D) has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below $V_{TC}$ threshold and 5/10 hours when the battery is higher than $V_{TC}$ threshold.

The user can program CC/CV charge safety timer through I2C (CHG_TIMER bits). When safety timer expires, the fault register CHRG_FAULT bits are set to 11 and an /INT is asserted to the host. The safety timer feature can be disabled through I2C by setting EN_TIMER bit.

During input voltage, current, JEITA cool/warm or thermal regulation, the safety timer will double as the setting value. The timer double function can be disable by writing 0 to TMR2X_EN bit.

During the fault (BAT_FAULT, NTC_FAULT), timer is suspended. Once the fault goes away, timer resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle CE pin or CHG_CFG bit).

### 10.6.2 NVDC Architecture

The SC89601(D) deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by VSYS_MIN bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 250mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, BATFET is fully on and the voltage difference between the system and battery is the $V_{DS}$ of BATFET.

When the battery charging is disabled and above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage. The status register VSYS_STAT bit goes high when the system is in minimum system voltage regulation.

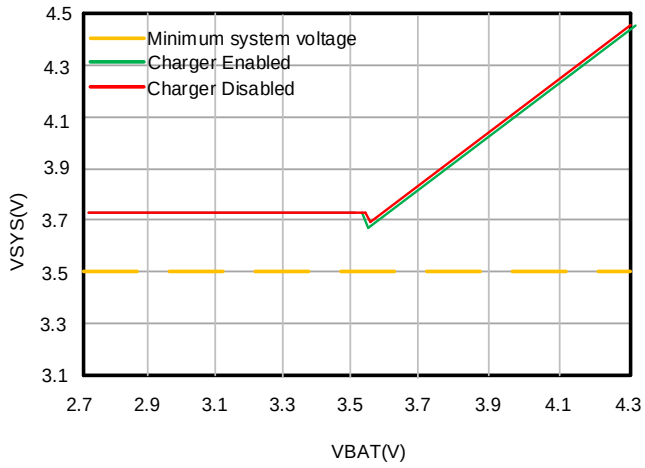



**Figure 5. System Voltage vs Battery Voltage**

### *10.6.2.1 Dynamic Power Management*

To meet maximum current limit in USB spec and avoid over loading the adapter, the device features Dynamic Power management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IIDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VINDPM_STAT or IINDPM_STAT goes high. Below figure shows the DPM response with 5V/2A adapter, 3.2V battery, 2.8A charge current and 3.5V minimum system voltage setting.

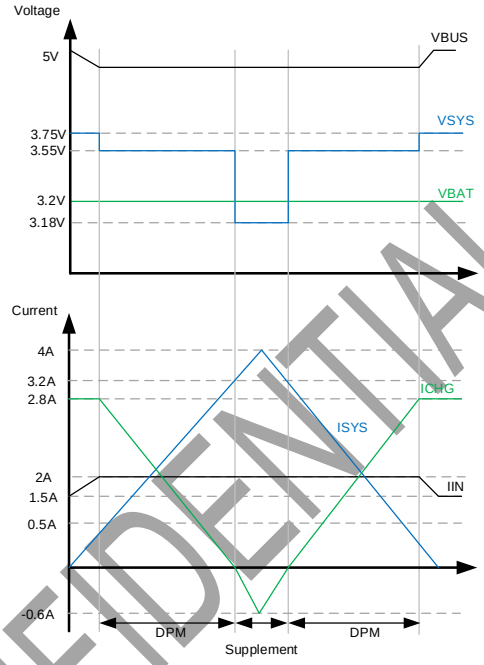



**Figure 6. DPM Response**

### *10.6.2.2 Supplement Mode*

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated the gate drive of BATFET so that the minimum BATFET $V_{DS}$ stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce $R_{DSON}$ until the BATFET is in full conduction. At this point onwards, the BATFET $V_{DS}$ linearly increases with discharge current. BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

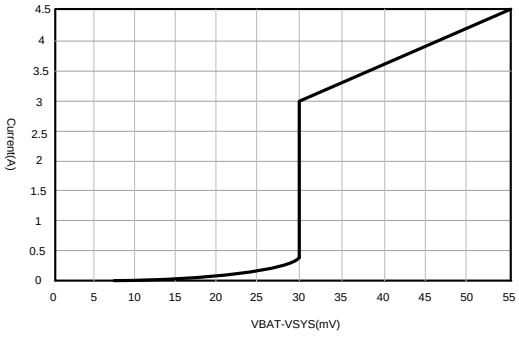



**Figure 7. BATFET V-I Curve**

## 10.7 Shipping Mode and /QON Pin

### 10.7.1 BATFET Disable Mode (Shipping Mode)

To extend battery life and minimize power when system is powered off during system idle, shipping, or storage, the device can turn off BATFET so that the system voltage is zero to minimize the battery leakage current. When the host set BATFET_DIS bit, the charger can turn off BATFET immediately or delay by $t_{SHIPMODE\_DLY}$ as configured by BATFET_DLY bit.

### 10.7.2 BATFET Enable(Exit Shipping Mode)

When the BATFET is disabled (in shipping mode) and indicated by setting BATFET_DIS, one of the following events can enable BATFET to restore system power:

1. Plug in adapter

2. Clear BATFET_DIS bit

3. Set REG_RST bit to reset all registers including BATFET_DIS bit to be default 0

4. A logic high to low transition on /QON pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit shipping mode

### 10.7.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plug-in. By changing the state of BATFET from on to off, systems connected to SYS can be effectively forced to have a power-on-reset. The /QON pin supports push-button interface to reset system power without host by changing the state of BATFET.

When the /QON pin is driven to logic low for $t_{QON\_RST}$ while input source is not plugged in and BATFET is enabled (BATFET_DIS = 0), the BATFET is turned off for $t_{BATFET\_RST}$ and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

### 10.7.4 /QON Pin Operations

The /QON pin incorporates two functions to control BATFET.

1. BATFET Enable: A /QON logic transition from high to low with longer than $t_{SHIPMODE}$ deglitch turns on BATFET and exit shipping mode.

2. BATFET Reset: When /QON is driven to logic low by at least $t_{QON\_RST}$ while adapter is not plugged in (and BATFET_DIS = 0), the BATFET is turned off for $t_{BATFET\_RST}$. The BATFET is re-enabled after $t_{BATFET\_RST}$ duration. This function allows systems connected to SYS to have power-on-reset. This function can be disabled by setting BATFET_RST_EN bit to 0.

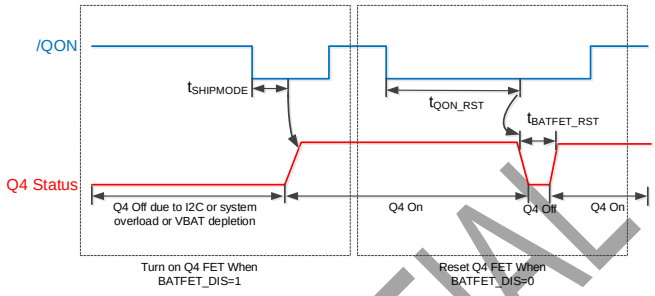



**Figure 8. SC89601(D) /QON Timing**

## 10.8 Power Good Indicator

The PG_STAT bit goes HIGH to indicate a good input source when:

- VBUS above $V_{VAC\_UVLO}$ below $V_{VAC\_OVP}$
- VBUS above VBAT+$V_{SLEEP}$ (not in sleep)
- VBUS above $V_{VBUSMIN}$ (typical 3.7V) when $I_{BADSRC}$ (typical 30 mA) current is applied (not a poor source)
- Completed input Source Type Detection

## 10.9 /INT

The SC89601(D) also has an alert mechanism that can output an interrupt signal via /INT to notify the system of the operation by outputting a 256μs low-state INT pulse. All the below events can trigger an /INT output:

- USB/adapter source identified
- Good input source detected as described in power good indicator
- Input Removed
- Charge Complete
- Enter and Exit top off timer
- VINDPM/IINDPM event detected (can be masked)
- Watchdog timer out, Safety timer out, OTG fault(VBUS overload, VBUS OVP, VBAT < $V_{BATLOW\_OTG}$), VBAT OVP, NTC COLD/HOT(Buck and Boost mode), Thermal shutdown, VAC OVP, VBUS<$V_{VBUSMIN}$

When a fault occurs, the charger device sends out /INT and keeps the fault state in REG until the host reads the fault register. The /INT signal can be masked when the corresponding control bit is set. When a fault/status change occurs, the charger device sends out an /INT pulse and keeps the state in REG09 until the host reads the registers. To read the current status, the host has to read REG09 two times

consecutively. The first read reports the pre-existing register status and the second read reports the current register status.

After the /INT 256us low state pulse, there has a 256us high state blocking time, if the /INT event occurs during the blocking time, the INT will send out the low state pulse after the blocking time. If the INT event occurs during the 256us low state, the INT will not send out the low state pulse but related state register still works.

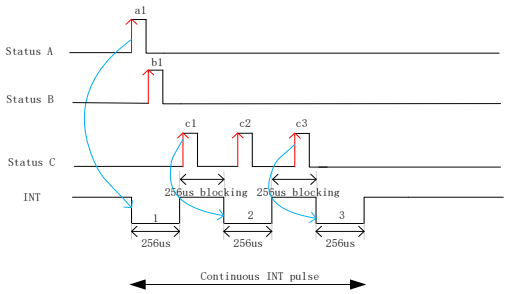



**Figure 9. /INT Pulse**

## 10.10 Protections

### 10.10.1 Voltage and Current Monitoring in Buck Mode

#### *10.10.1.1 Input Over voltage (ACOVP)*

If VBUS voltage exceeds $V_{VAC\_OV}$ (programmable via VAC_OVP[2:0] bits), the device stops switching immediately. During input over voltage event (ACOV), the fault register CHRG_FAULT bits are set to 01. An /INT pulse is asserted to the host. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold.

#### *10.10.1.2 System Over Voltage Protection (VSYSOVP)*

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 106% above target VSYS. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger provides 30mA discharge current to bring down the system voltage.

### 10.10.2 Voltage and Current Monitoring in Boost Mode

#### *10.10.2.1 VBUS Soft Start*

When the boost function is enabled, the device soft-starts boost mode to avoid inrush current.

#### *10.10.2.2 VBUS Over Load Protection*

The device monitors boost output voltage and other conditions to provide output short circuit and over voltage protection. The Boost build in accurate constant current regulation to allow OTG to adaptive to various types of load. If short circuit is detected on VBUS, the Boost turns off and retry 7 times. If retries are not successful, OTG is disabled with OTG_CFG bit cleared. In addition, the BOOST_FAULT bit is set and /INT pulse is generated. The BOOST_FAULT bit can be cleared by host by re-enabling boost mode.

#### *10.10.2.3 VBUS Over Voltage Protection*

When the VBUS voltage rises above regulation target and exceeds $V_{OTG\_OVP}$, the device enters over voltage protection which stops switching, clears OTG_CFG bit and exits boost mode. At Boost over voltage duration, the fault register bit (BOOST_FAULT) is set high to indicate fault in boost operation. An INT is also asserted to the host.

### 10.10.3 Thermal Regulation and Thermal Shutdown

#### *10.10.3.1 Thermal Protection in Buck Mode*

The SC89601(D) monitors the internal junction temperature $T_J$ to avoid overheat the chip and limits the IC surface temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds $T_{SHUT}$(150°C). The fault register CHRG_FAULT is set to 1 and an INT is asserted to the host. The BATFET and converter is enabled to recover when IC temperature is $T_{SHUT\_HYS}$ (30°C) below $T_{SHUT}$(150°C).

#### *10.10.3.2 Thermal Protection in Boost Mode*

The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds $T_{SHUT}$ (150°C), the boost mode is disabled by setting OTG_CFG bit low. When IC junction temperature is below $T_{SHUT}$(150°C) - $T_{SHUT\_HYS}$ (30°C), the BATFET is enabled automatically to allow system to restore and the host can re-enable OTG_CFG bit to recover.

#### 10.10.4 Battery Protection

##### *10.10.4.1 Battery Over voltage Protection (VBATOVP)*

The battery overvoltage limit is clamped at 4% above the battery regulation voltage. When battery over voltage occurs, the charger device immediately disables charging. The fault register BAT_FAULT bit goes high and an /INT is asserted to the host.

##### *10.10.4.2 Battery Over discharge Protection*

When battery is discharged below $V_{BAT\_DPL}$, the BATFET is turned off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VBUS. The battery is charged with $I_{SHORT}$ (typically 50mA) current when the VBAT < $V_{BAT\_SHORT}$.

##### *10.10.4.3 System Over current Protection*

When the system is shorted or significantly overloaded (IBAT > $I_{BATOCP}$ for 100us deglitch) so that the current exceeds BATFET over current limit, the BATFET latches off. Set BATFET Enable (Exit Shipping Mode) can reset the latch-off condition and turn on BATFET.

### 10.11 I2C Interface

#### 10.11.1 I2C Interface

The IC features I2C interface, so the MCU or controller can control the IC flexibly. The 7-bit I2C address of the chip is 0x6B(SC89601(D)). The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The I2C interface supports both standard mode (up to 100kbits) and fast mode (up to 400k bits with 5 kΩ pull up resistor at SCL pin and SDA pin respectively).

#### 10.11.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

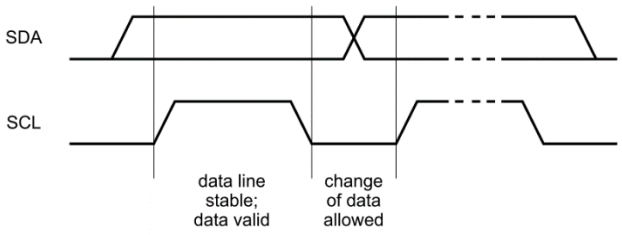



**Figure 10. Bit transfer on the I2C bus**

#### 10.11.3 START and STOP Conditions

All transactions begin with a START (S) and are terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

START and STOP conditions are always generated by the master. The bus is busy after the START condition. The bus is free again a certain time after the STOP condition.

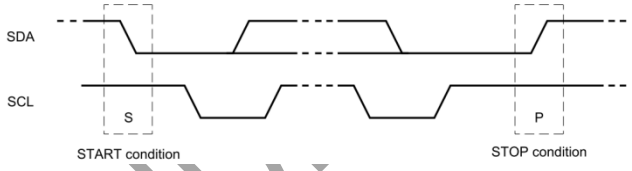



**Figure 11. START and STOP conditions**

#### 10.11.4 Byte Format

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte must be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, for example servicing an internal interrupt, it can hold the clock line SCL LOW to force the master into a wait state. Data transfer then continues when the slave is ready for another byte of data and releases clock line SCL.

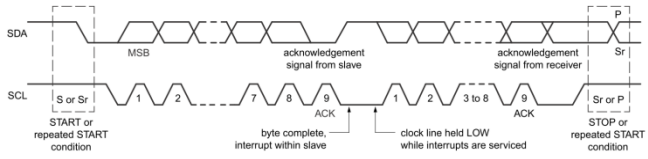



**Figure 12. Data transfer on the I2C bus**

#### 10.11.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. During data is transferred, the master can either be the transmitter or the receiver. No matter what it is, the master generates all clock pulses, including the acknowledge ninth clock pulse.

The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it

remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during this ninth clock pulse, this is defined as the Not Acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer.

### 10.11.6 The slave address and R/W bit

Data transfers follow the format shown in below. After the START condition (S), a slave address is sent. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W) — a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

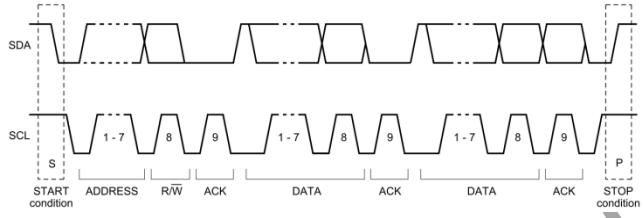



**Figure 13. complete data transfer**

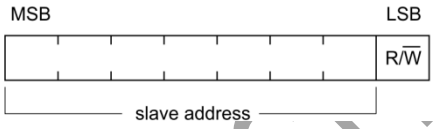



**Figure 14. The first byte after the START procedure**

### 10.11.7 Single Read and Write

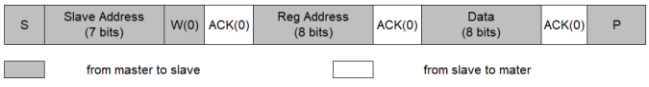



**Figure 15. Single Write**

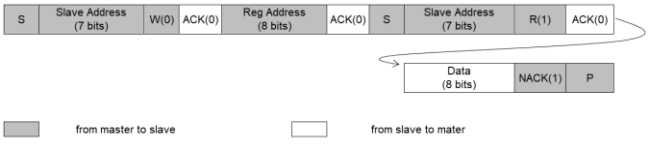



**Figure 16. Single Read**

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

### 10.11.8 Multi-Read and Multi-Write

The IC supports multi-read and multi-write for continuous registers.

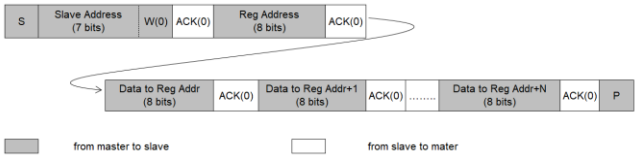



**Figure 17. Multi-Write**

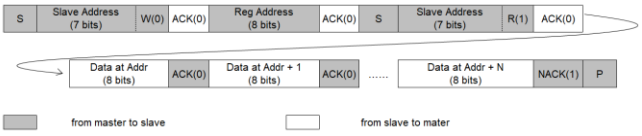



**Figure 18. Multi-Read**

# 11 Application information (TBD)

## 12 Register Map

| ADDR | Name | R/W | Default | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00H | IINDPM | RW | 00000100 | EN_HIZ | EN_STAT_PIN | | IINDPM | | | | |
| 01H | CTL1 | RW | 00011010 | PFM_DIS | WD_RST | OTG_CFG | CHG_CFG | VSYS_MIN | | | VBATLOW_OTG |
| 02H | ICC | RW | 1X100010 | BOOST_LIM | Reserved | ICC | | | | | |
| 03H | ITC&ITERM | RW | 00100010 | ITC | | | | ITERM | | | |
| 04H | VBAT_REG | RW | 01011000 | VBAT_REG | | | | | TOP OFF TIMER | | VRECHG |
| 05H | CTL2 | RW | 10011111 | EN_TERM | Reserved | TWD | | EN_TIMER | CHG_TIMER | TREG | JEITA_COOL_ISET |
| 06H | VINDPM&BOOSTV&OVP | RW | 01100110 | VAC_OVP | | BOOSTV[2:1] | | VINDPM | | | |
| 07H | CTL3 | RW | 01000100 | FORCE_DPDM (PSEL) | TMR2X_EN | BATFET_DIS | JEITA_WARM_VSET1 | BATFET_DLY | BATFET_RST_EN | VINDPM_TRACK | |
| 08H | STAT1 | R | XXXXXXXX | VBUS_STAT | | | CHRG_STAT | | PG_STAT | THERM_STAT | VSYS_STAT |
| 09H | FAULT | R | XXXXXXXX | WD_FAULT | BOOST_FAULT | CHRG_FAULT | | BAT_FAULT | NTC_FAULT | | |
| 0AH | STAT2 | RW | XXXXXX00 | VBUS_GD | VINDPM_STAT | IINDPM_STAT | CV_STAT | TOP OFF ACTIVE | ACOV_STAT | VINDPM_INT_MASK | IINDPM_INT_MASK |
| 0BH | REG_RST&DEV&PN | RW | 00011X00 | REG_RST | PN | | | | Reserved | DEV_VERSION | |
| 0CH | JEITA | RW | 00110101 | JEITA_COOL_ISET2 | JEITA_WARM_VSET2 | JEITA_WARM_ISET | | JEITA_COOL_TEMP | | JEITA_WARM_TEMP | |
| 0DH | CTL4 | RW | 00100100 | VBAT_REG_FT | | BOOST_NTC_HOT_TEMP | | BOOST_NTC_COLD_TEMP | BOOSTV [3] | BOOSTV [0] | ISHORT |
| 0EH | CTL5 | RW | 1X110010 | VTC | INPUT_DET_DONE | AUTO_DPDM_EN | BUCK_FREQ | BOOST_FREQ | VSYSOVP | | NTC_DIS |

## 12.1 REG 00H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R/W | EN_HIZ | 0 | Y | Y | Enable HI-Z Mode<br>0: Disable<br>1: Enable | Register bits are reset to default value when input source is plug-in. |
| 6 | R/W | EN_STAT_PIN | 0 | Y | N | 00: Enable STAT Pin Function<br>01：Reserved<br>10：Reserved<br>11：Disable STAT Pin Function | |
| 5 | R/W | | 0 | Y | N | | |
| 4 | R/W | IINDPM | 0 | Y | N | 1600mA | Input current limit<br>Offset: 100 mA<br>Range: 100 mA (000000) – 3.2A (11111) |
| 3 | R/W | | 0 | Y | N | 800mA | |
| 2 | R/W | | 1 | Y | N | 400mA | |
| 1 | R/W | | 0 | Y | N | 200mA | |
| 0 | R/W | | 0 | Y | N | 100mA | |

## 12.2 REG 01H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R/W | PFM_DIS | 0 | Y | N | 0: Enable PFM<br>1: Disable PFM | |
| 6 | RW1C | WD_RST | 0 | Y | Y | 0: Normal<br>1: Reset | |
| 5 | R/W | OTG_CFG | 0 | Y | Y | 0: OTG Disable<br>1: OTG Enable | |
| 4 | R/W | CHG_CFG | 1 | Y | Y | 0: Charge Disable<br>1: Charge Enable | |
| 3 | R/W | VSYS_MIN | 1 | Y | N | 000:2.6V<br>001:2.8V<br>010:3.0V<br>011:3.2V<br>100:3.4V<br>101:3.5V<br>110:3.6V<br>111:3.7V | |
| 2 | R/W | | 0 | Y | N | | |
| 1 | R/W | | 1 | Y | N | | |
| 0 | R/W | VBATLOW_OTG | 0 | Y | N | 0: 2.8V<br>1: 2.5V | |

## 12.3 REG 02H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R/W | BOOST_LIM | 1 | Y | Y | 0: 0.5A<br>1: 1.2A | |
| 6 | R/W | Reserved | | | | | |
| 5 | R/W | ICC | 1 | Y | Y | 1920mA | CC charge current:<br>Default: 2040mA (100010)<br>Range: 0 mA (0000000) – 3000 mA (110010)<br>Note:<br>ICHG = 0 mA disable charge.<br>ICHG > 3000 mA (110010) clamped to register value 3000 mA (110010) |
| 4 | R/W | | 0 | Y | Y | 960mA | |
| 3 | R/W | | 0 | Y | Y | 480mA | |
| 2 | R/W | | 0 | Y | Y | 240mA | |
| 1 | R/W | | 1 | Y | Y | 120mA | |
| 0 | R/W | | 0 | Y | Y | 60mA | |

## 12.4 REG 03H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R/W | ITC | 0 | Y | Y | 480mA | Trickle Current Limit<br>Offset: 60mA<br>Range: 60mA – 960mA<br>Default: 180mA (0010) |
| 6 | R/W | | 0 | Y | Y | 240mA | |
| 5 | R/W | | 1 | Y | Y | 120mA | |
| 4 | R/W | | 0 | Y | Y | 60mA | |
| 3 | R/W | ITERM | 0 | Y | Y | 480mA | Termination Current Limit<br>Offset: 60mA<br>Range: 60mA – 960mA<br>Default: 180mA (0010) |
| 2 | R/W | | 0 | Y | Y | 240mA | |
| 1 | R/W | | 1 | Y | Y | 120mA | |
| 0 | R/W | | 0 | Y | Y | 60mA | |

## 12.5 REG 04H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R/W | VBAT_REG | 0 | Y | Y | 512mV | Charge Voltage Limit<br>Offset: 3.848V<br>Range: 3.848V-4.864V<br>Default: 4.2V (01011)<br>VBAT_REG also can be adjusted through VBAT_REG_FT |
| 6 | R/W | | 1 | Y | Y | 256mV | |
| 5 | R/W | | 0 | Y | Y | 128mV | |
| 4 | R/W | | 1 | Y | Y | 64mV | |
| 3 | R/W | | 1 | Y | Y | 32mV | |
| 2 | R/W | TOP OFF TIMER | 0 | Y | Y | 00: Disable;<br>01: 15mins;<br>10: 30mins;<br>11:45mins | |
| 1 | R/W | | 0 | Y | Y | | |
| 0 | R/W | VRECHG | 0 | Y | Y | 0:100mV<br>1:200mV | |

## 12.6 REG 05H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R/W | EN_TERM | 1 | Y | Y | Charging Termination Enable<br>0 – Disable<br>1 – Enable (default) | |
| 6 | R/W | Reserved | | | | | |
| 5 | R/W | $T_{WD}$ | 0 | Y | Y | I2C Watchdog Timer Setting<br>00 – Disable watchdog timer<br>01 – 40s (default)<br>10 – 80s<br>11 – 160s | |
| 4 | R/W | | 1 | Y | Y | | |
| 3 | R/W | EN_TIMER | 1 | Y | Y | Charging Safety Timer Enable<br>0 – Disable<br>1 – Enable (default) | |
| 2 | R/W | CHG_TIMER | 1 | Y | Y | 0:5hrs<br>1:10hrs | |
| 1 | R/W | TREG | 1 | Y | Y | 0.90°C<br>1:110°C | |
| 0 | R/W | JEITA_COOL_ISET1 | 1 | Y | Y | 0: 50% of ICC<br>1: 20% of ICC (default) | |

## 12.7 REG 06H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R/W | VAC_OVP | 0 | Y | N | 00 :5.8V<br>01: 6.4 V<br>10: 11V<br>11: 14.2 V | |
| 6 | R/W | | 1 | Y | N | | |
| 5 | R/W | BOOSTV [2] | 1 | Y | N | 400mV | Offset:3.9V<br>Default: 5.1V<br>BOOSTV = Offset + 100mV x BOOSTV[0:3] |
| 4 | R/W | BOOSTV [1] | 0 | Y | N | 200mV | |
| 3 | R/W | VINDPM | 0 | Y | N | 800mV | Absolute VINDPM Threshold<br>Offset: 3.9 V<br>Range: 3.9 V (0000) – 5.1 V (1100)<br>Default: 4.5V (0110)<br>Special value:<br>1111: 8.4V<br>1110: 8.2V<br>1101: 8V<br>Register bits are reset to default value when input source is plug-in |
| 2 | R/W | | 1 | Y | N | 400mV | |
| 1 | R/W | | 1 | Y | N | 200mV | |
| 0 | R/W | | 0 | Y | N | 100mV | |

## 12.8 REG 07H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | RW1C | FORCE_DPDM(PSEL) | 0 | Y | Y | Force DP/DM(PSEL) Detection<br>0 – Not in DP/DM(PSEL) detection (default)<br>1 – Force DP/DM(PSEL) detection | |
| 6 | R/W | TMR2X_EN | 1 | Y | Y | Safety Timer Setting during DPM or Thermal Regulation<br>0 – Safety timer not slowed by 2X during input DPM or thermal regulation or JEITA<br>1 – Safety timer slowed by 2X during input DPM or thermal regulation or JEITA (default) | |
| 5 | R/W | BATFET_DIS | 0 | Y | N | 0: Allow Q4 turn on<br>1: Turn off Q4 | Register bits are reset to default value when input source is plug-in. |
| 4 | R/W | JEITA_WARM_VSET1 | 0 | Y | Y | 0: VREG-200mV<br>1: VREG | |
| 3 | R/W | BATFET_DLY | 0 | Y | N | 0: Turn off BATFET immediately when BATFET_DIS bit is set<br>1: Turn off BATFET after $t_{SHIPMODE\_DLY}$ (typ.10s) when BATFET_DIS bit is set | |
| 2 | R/W | BATFET_RST_EN | 1 | Y | Y | 0: Disable BATFET reset function<br>1: Enable BATFET reset function | |
| 1 | R/W | VINDPM_TRACK | 0 | Y | N | 00: Disable;<br>01: VBAT+200mV;<br>10: VBAT+250mV;<br>11: VBAT+300mV | Register bits are reset to default value when input source is plug-in. |
| 0 | R/W | | 0 | Y | N | | |

## 12.9 REG 08H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R | VBUS_STAT | X | NA | NA | VBUS Status register<br>000: No Input<br>001: USB Host SDP<br>010: USB CDP (1.5A)<br>011: USB DCP (2.4A)<br>100: Reserved<br>101: Unknown Adapter (500mA)<br>110: Non-Standard Adapter (1A/2A/2.1A/2.4A)<br>111: OTG | |
| 6 | R | | X | NA | NA | | |
| 5 | R | | X | NA | NA | | |
| 4 | R | CHRG_STAT | X | NA | NA | Charging status:<br>00: Not Charging<br>01: TC-charge (< $V_{TC}$)<br>10: Fast Charging<br>11: Charge Termination | |
| 3 | R | | X | NA | NA | | |
| 2 | R | PG_STAT | X | NA | NA | Power Good status:<br>0: Power Not Good<br>1: Power Good | |
| 1 | R | THERM_STAT | X | NA | NA | 0: Not in thermal loop<br>1: In thermal loop | |
| 0 | R | VSYS_STAT | X | NA | NA | 0: Not in VSYSMIN regulation<br>1: In VSYSMIN regulation | |

## 12.10 REG 09H

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R | WD_FAULT | X | NA | NA | 0: Normal<br>1: Watchdog timer expiration | |
| 6 | R | BOOST_FAULT | X | NA | NA | 0: Normal<br>1: VBUS overloaded in OTG, or VBUS OVP, or battery is too low (any conditions that we cannot start boost function) | |
| 5 | R | CHRG_FAULT | X | NA | NA | 00: Normal;<br>01: Input fault (VAC OVP or VBAT < VBUS < 3.8 V);<br>10: Thermal shutdown;<br>11: Charge Safety Timer Expiration | |
| 4 | R | | X | NA | NA | | |
| 3 | R | BAT_FAULT | X | NA | NA | 0: Normal<br>1: BATOVP | |
| 2 | R | NTC_FAULT | X | NA | NA | NTC Fault Status<br>Buck Mode:<br>000 – Normal<br>010 – TS Warm<br>011 – TS Cool<br>101 – TS Cold<br>110 – TS Hot<br>Boost Mode:<br>000 – Normal<br>101 – TS Cold<br>110 – TS Hot | |
| 1 | R | | X | NA | NA | | |
| 0 | R | | X | NA | NA | | |

## 12.11 REG 0AH

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | R | VBUS_GD | X | NA | NA | 0: VBUS Not Attached<br>1: VBUS Attached | |
| 6 | R | VINDPM_STAT | X | NA | NA | 0: Not in VIINDPM LOOP<br>1: In VINDPM LOOP | |
| 5 | R | IINDPM_STAT | X | NA | NA | 0: Not in IIINDPM LOOP<br>1: In IINDPM LOOP | |
| 4 | R | CV_STAT | X | NA | NA | 0: Not in CV LOOP<br>1: In CV LOOP | |
| 3 | R | TOP OFF ACTIVE | X | NA | NA | 0: Top off Timer not Counting<br>1: Top off Timer Counting | |
| 2 | R | ACOV_STAT | X | NA | NA | 0: Not in VAC OVP<br>1: In VAC OVP | |
| 1 | R/W | VINDPM_INT_MASK | 0 | Y | N | 0: Allow VINDPN INT PULSE<br>1: Mask VINDPM INT PULSE | |
| 0 | R/W | IINDPM_INT_MASK | 0 | Y | N | 0: Allow IINDPN INT PULSE<br>1: Mask IINDPM INT PULSE | |

## 12.12 REG 0BH

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | RW1C | REG_RST | 0 | NA | NA | Register Reset<br>0 – Keep current register setting (default)<br>1 – Reset to default register value and reset safety timer | |
| 6 | R | PN | 0 | NA | NA | 0011: SC89601(D) | |
| 5 | R | | 0 | NA | NA | | |
| 4 | R | | 1 | NA | NA | | |
| 3 | R | | 1 | NA | NA | | |
| 2 | R | Reserved | X | NA | NA | | |
| 1 | R | DEV_VERSION | 0 | NA | NA | | |
| 0 | R | | 0 | NA | NA | | |

## 12.13 REG 0CH

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | RW | JEITA_COOL_ISET2 | 0 | Y | Y | CC current setting during cool temperature range, as percentage of ICC<br>0: Depend on JEITA_COOL_ISET1<br>1: 100% of ICC (JEITA_COOL_ISET1 = 0)<br>No charge (JEITA_COOL_ISET1 = 1) | |
| 6 | RW | JEITA_WARM_VSET2 | 0 | Y | Y | Warm charge voltage setting<br>0: Depend on JEITA_WARM_VSET1<br>1: VREG - 100mV (JEITA_WARM_VSET1 = 0)<br>VREG -50mV (JEITA_WARM_VSET1 = 1) | |
| 5 | RW | JEITA_WARM_ISET | 1 | Y | Y | CC charge current setting during warm temperature range as percentage of ICC<br>00 – No Charge<br>01 – 20% of ICC<br>10 – 50% of ICC<br>11 – 100% of ICC (default) | |
| 4 | RW | | 1 | Y | Y | | |
| 3 | RW | JEITA_COOL_TEMP | 0 | Y | Y | 00 = 70.75% (5°C)<br>01 = 68.25% (10°C) (default)<br>10 = 65.25% (15°C)<br>11 = 62.25% (20°C) | |
| 2 | RW | | 1 | Y | Y | | |
| 1 | RW | JEITA_WARM_TEMP | 0 | Y | Y | 00 = 48.25% (40°C)<br>01 = 44.75% (44.5°C) (default)<br>10 = 40.75% (50.5°C)<br>11 = 37.75% (54.5°C) | |
| 0 | RW | | 1 | Y | Y | | |

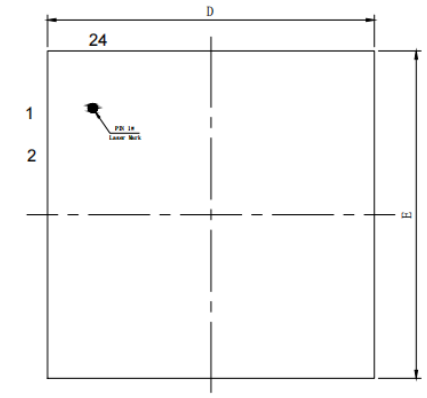
## 12.14 REG 0DH

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | RW | VBAT_REG_FT | 0 | Y | Y | 00: VBAT_REG<br>01: VBAT_REG+8mV<br>10: VBAT_REG+16mV<br>11: VBAT_REG+24mV | VBAT_REG fine tuning. |
| 6 | RW | | 0 | Y | Y | | |
| 5 | RW | BOOST_NTC_HOT_TEMP | 1 | Y | Y | 00:37.75%;<br>01:34.75%;<br>10:31.25%;(default)<br>11: REV | |
| 4 | RW | | 0 | Y | Y | | |
| 3 | RW | BOOST_NTC_COLD_TEMP | 0 | Y | Y | 0:80%(default)<br>1:77% | |
| 2 | RW | BOOSTV[3] | 1 | Y | N | 800mV | Offset: 3.9V<br>Default: 5.1V<br>BOOSTV = Offset + 100mV x BOOSTV[0:3] |
| 1 | RW | BOOSTV[0] | 0 | Y | N | 100mV | |
| 0 | RW | ISHORT | 0 | Y | N | 0: 50mA<br>1: 90mA | |

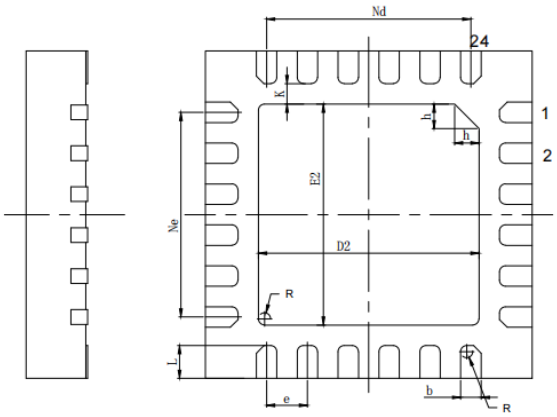
## 12.15 REG 0EH

| Bit | Type | Bit Name | POR | Reset by REG_RST | Reset by WDT | Description | Notes |
|---|---|---|---|---|---|---|---|
| 7 | RW | VTC | 1 | Y | N | TC to CC Threshold:<br>0: 3V<br>1: 2.8V | |
| 6 | R | INPUT_DET_DONE | x | NA | NA | 0: Normal<br>1: DPDM Detection Done | |
| 5 | RW | AUTO_DPDM_EN | 1 | Y | N | Automatic DP/DM Detection Control<br>0 –Disable DP/DM detection when VBUS is plugged in<br>1 –Enable DP/DM detection when VBUS is plugged in (default) | |
| 4 | RW | BUCK_FREQ | 1 | Y | Y | 0: 1MHz<br>1: 1.5MHz | |
| 3 | RW | BOOST_FREQ | 0 | Y | Y | Boost Mode Frequency Selection<br>0 – 1.5MHz<br>1 – 500KHz<br>Note: Write to this bit is ignored when OTG_CFG is enabled. | |
| 2 | RW | VSYSOVP | 0 | Y | Y | 00: 104%<br>01: 106%<br>10: 108%<br>11: 110% | |
| 1 | RW | | 1 | Y | Y | | |
| 0 | RW | NTC_DIS | 0 | Y | N | 0: Include NTC pin into charger and boost mode function<br>1: Ignore NTC pin. Always consider NTC is good to allow charging and boost mode. | |

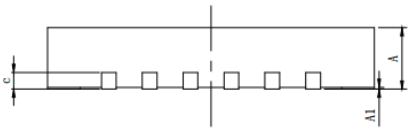
## 13 MECHANICAL DATA




TOP VIEW



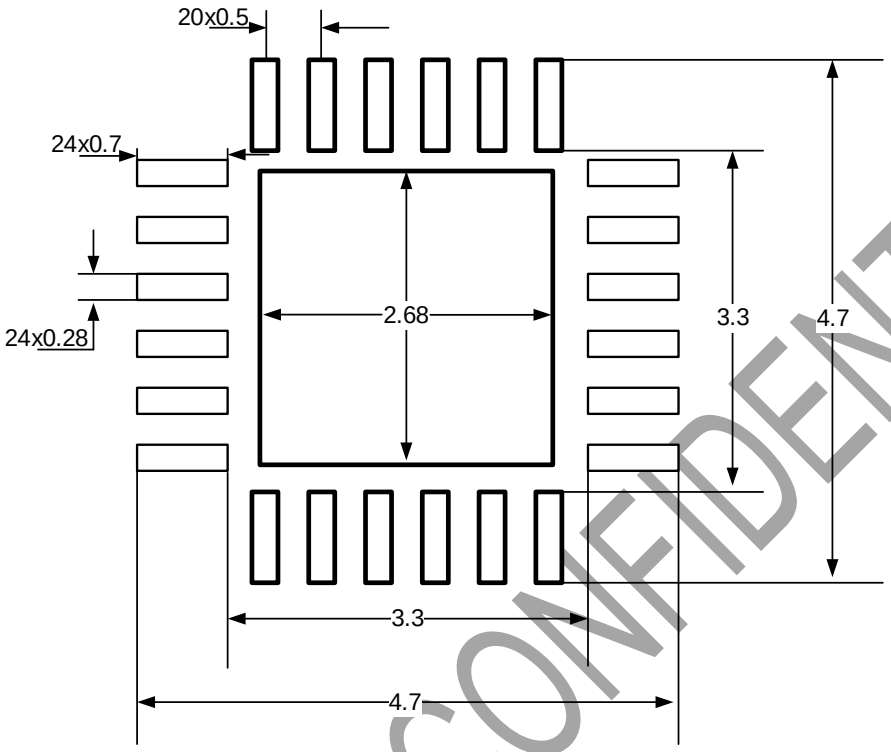

BOTTOM VIEW




SIDE VIEW

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0 | 0.02 | 0.05 |
| b | 0.20 | 0.25 | 0.30 |
| c | | 0.203REF | |
| D | 3.90 | 4.00 | 4.10 |
| D2 | 2.60 | 2.70 | 2.80 |
| e | | 0.50BSC | |
| Nd | | 2.50BSC | |
| Ne | | 2.50BSC | |
| E | 3.90 | 4.00 | 4.10 |
| E2 | 2.60 | 2.70 | 2.80 |
| L | 0.35 | 0.40 | 0.45 |
| h | 0.25 | 0.30 | 0.35 |
| K | | 0.25REF | |
| R | | 0.075REF | |

**RECOMMENDED FOOTPRINT (Unit mm)**



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